MINIMIZING TRANSISTOR VARIATIONS DUE TO SHALLOW TRENCH ISOLATION STRESS

ABSTRACT OF THE DISCLOSURE

The present invention provides, in one embodiment, a method of manufacturing a Metal Oxide Semiconductor transistor (100). The method comprises forming an active area (105) in a substrate (115), wherein the active area (105) is bounded by an isolation structure (120). The method further includes placing at least one stress adjustor (130) adjacent the active area (105), wherein the stress adjustor (130) is positioned to modify a mobility of a majority carrier within a channel region (155) of the MOS transistor (100).

Other embodiments of the present invention include a MOS transistor device (200) and a process (300) for constructing an integrated circuit.